

AUTOMATED GENERATION OF BUILT-IN SELF-TEST AND MEASUREMENT CIRCUITRY FOR MIXED-SIGNAL CIRCUITS AND SYSTEMS

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Overview

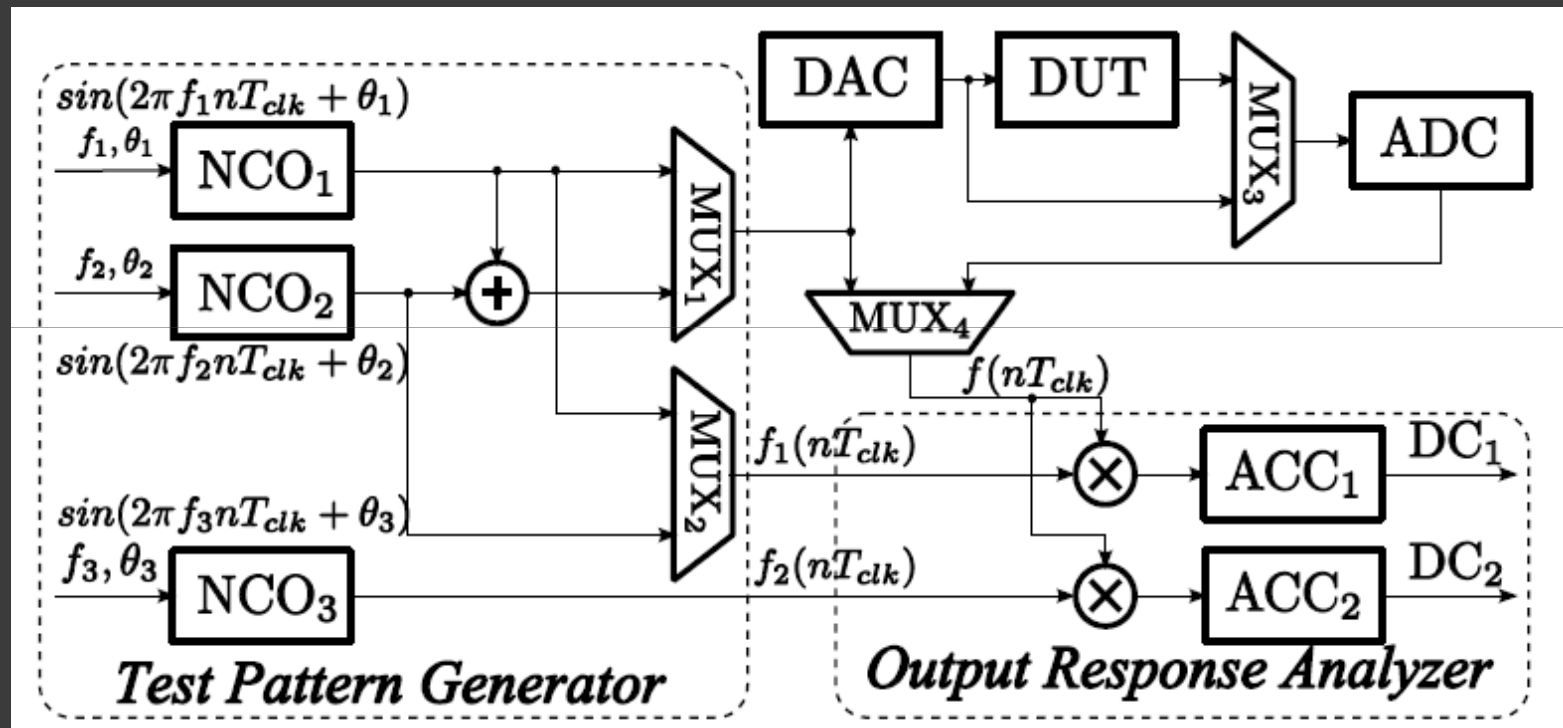
- ⦿ Goals
- ⦿ Model Design
 - Top Level Architecture
- ⦿ Program
 - VHDL Generation
 - Example Implementations
- ⦿ Experimental Results
- ⦿ Summary

Goals

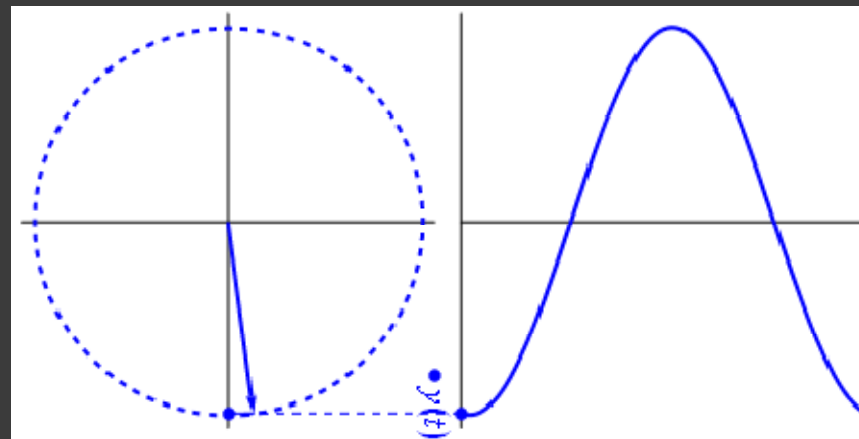
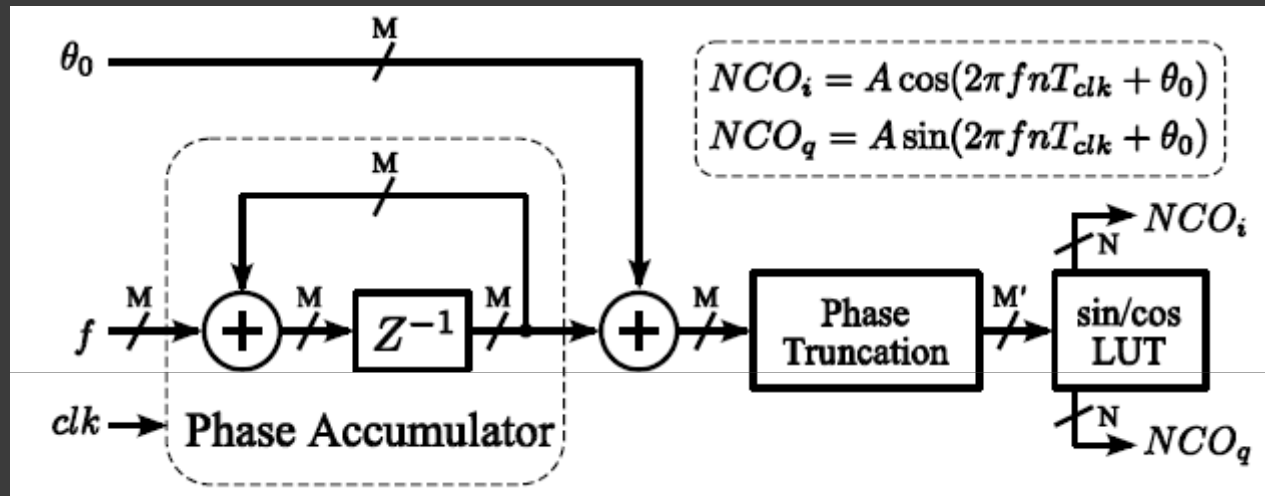
- ⦿ Perform on chip calculations of:
 - Linearity
 - Frequency Response
 - Noise Figure

Built-In Self-Test
BIST

Top Level Architecture



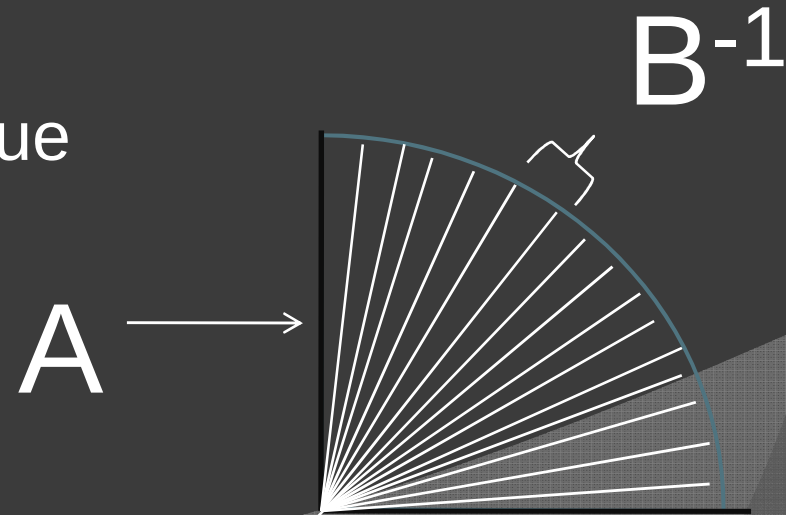
Numerically Controlled Oscillator



Sin/Cos Table Generation

⊙ $\text{TableEntry} = A * \sin(3.141592 * I / (2 * B))$

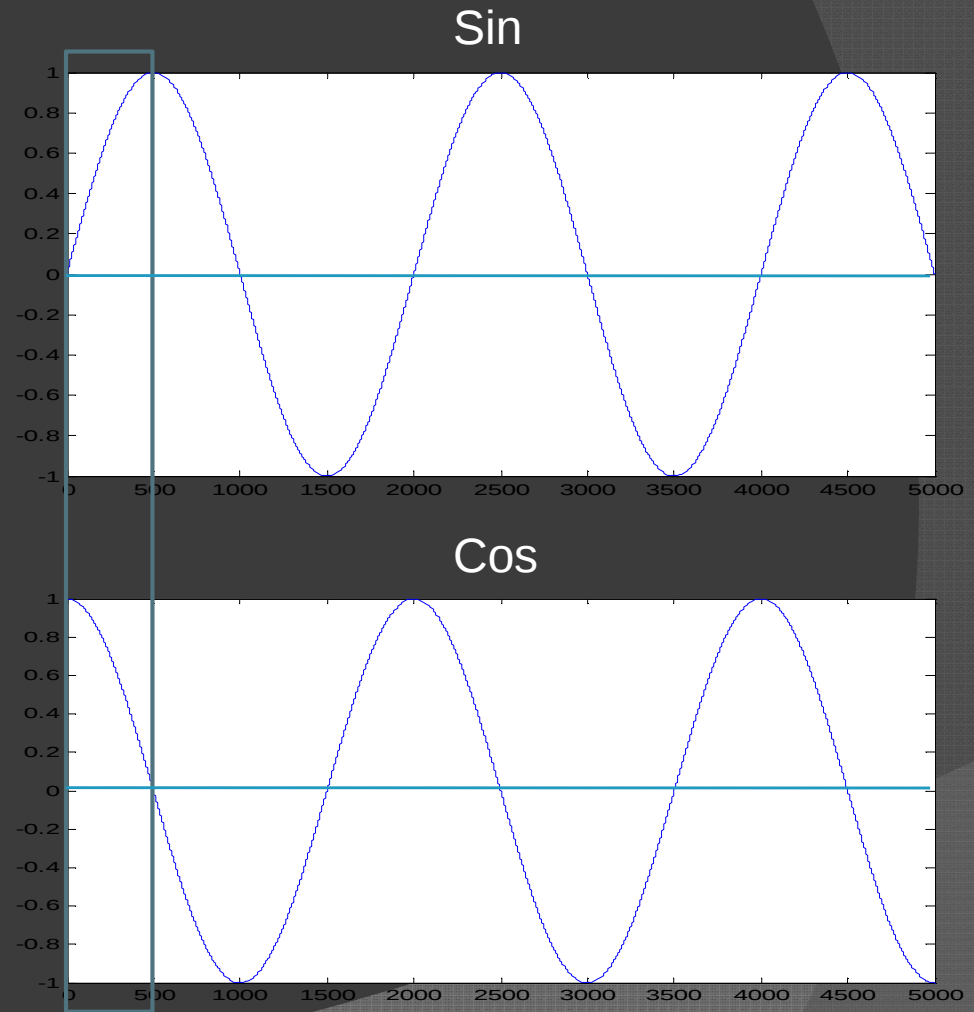
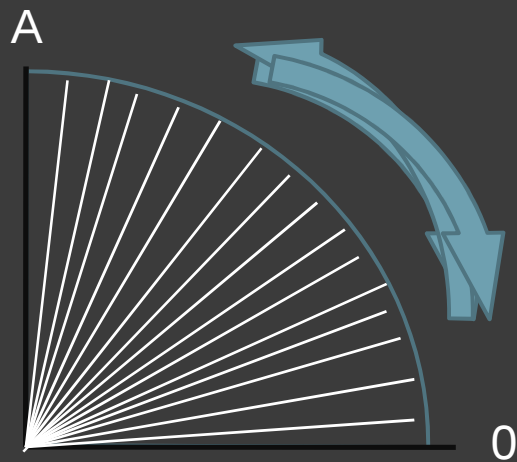
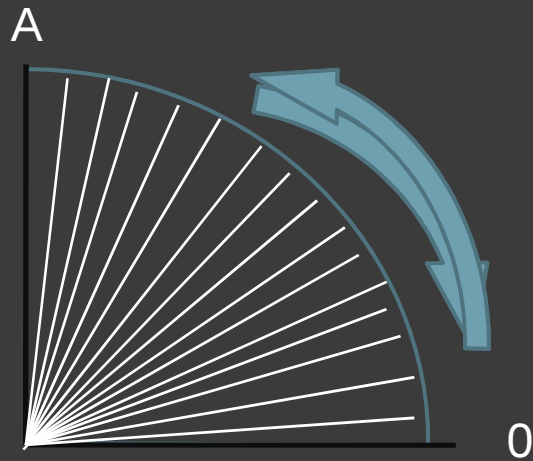
- A is the magnitude of the output
 - $A = 2^{\text{\#of magnitude bits}-1}$
- B is the number of entries in the table
 - $B = \text{\#of table entries}$
- I is the table index value



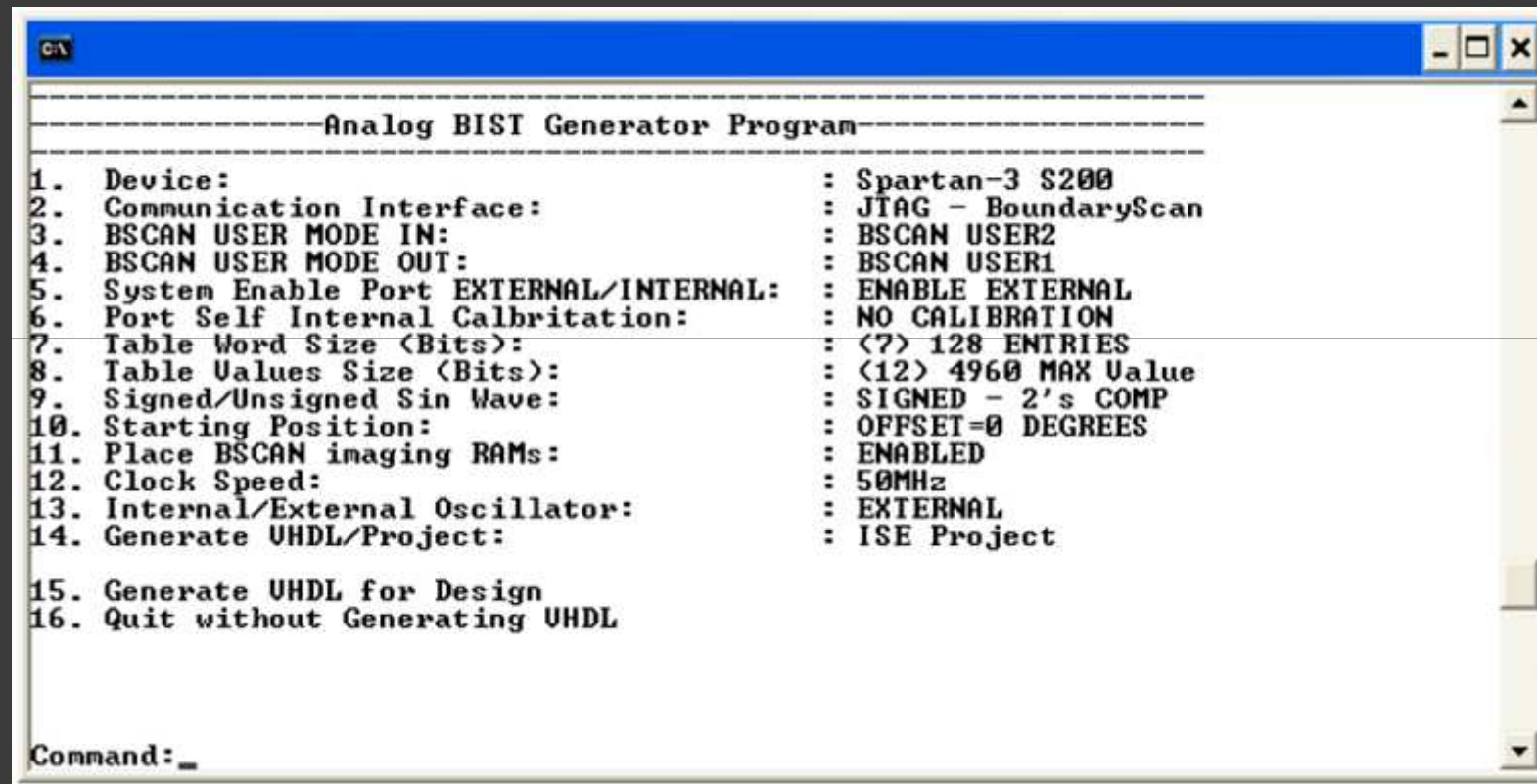
Lookup Table

```
case table_index is
  when 0 =>
    table_value := 0;
  when 1 =>
    table_value := 1304;
  when 2 =>
    table_value := 2401;
  when 3 =>
    table_value := 3001;
  .....
```

Generating waveforms



VHDL Generation

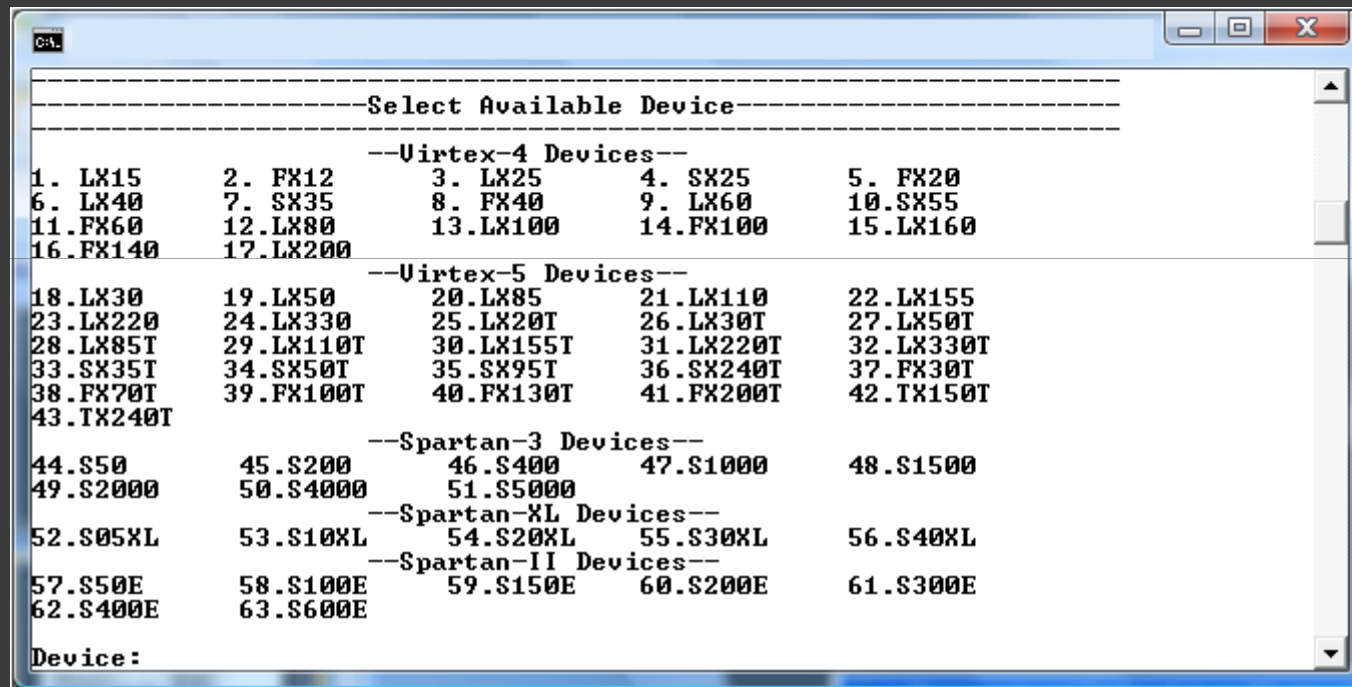


```
-----Analog BIST Generator Program-----
1. Device:                               : Spartan-3 S200
2. Communication Interface:              : JTAG - BoundaryScan
3. BSCAN USER MODE IN:                  : BSCAN USER2
4. BSCAN USER MODE OUT:                 : BSCAN USER1
5. System Enable Port EXTERNAL/INTERNAL: : ENABLE EXTERNAL
6. Port Self Internal Calbritation:      : NO CALIBRATION
7. Table Word Size <Bits>:               : <7> 128 ENTRIES
8. Table Values Size <Bits>:            : <12> 4960 MAX Value
9. Signed/Unsigned Sin Wave:            : SIGNED - 2's COMP
10. Starting Position:                  : OFFSET=0 DEGREES
11. Place BSCAN imaging RAMs:           : ENABLED
12. Clock Speed:                       : 50MHz
13. Internal/External Oscillator:       : EXTERNAL
14. Generate VHDL/Project:              : ISE Project

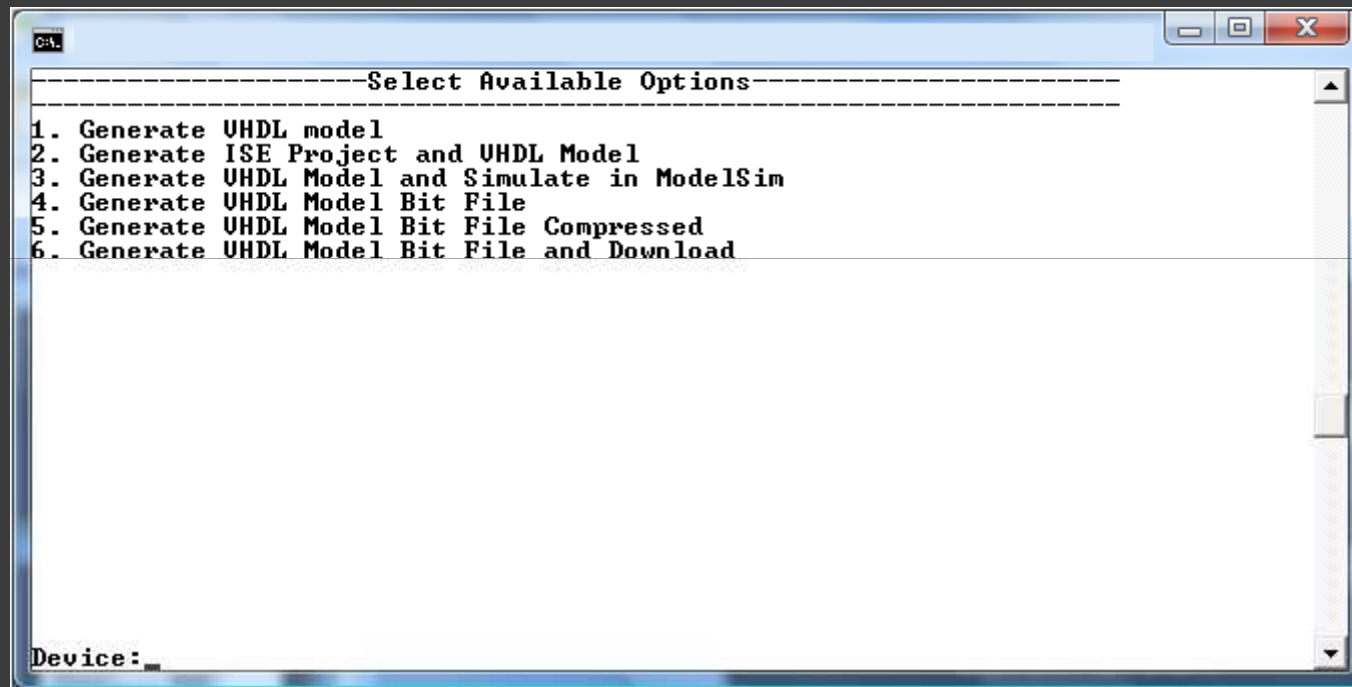
15. Generate VHDL for Design
16. Quit without Generating VHDL

Command: _
```

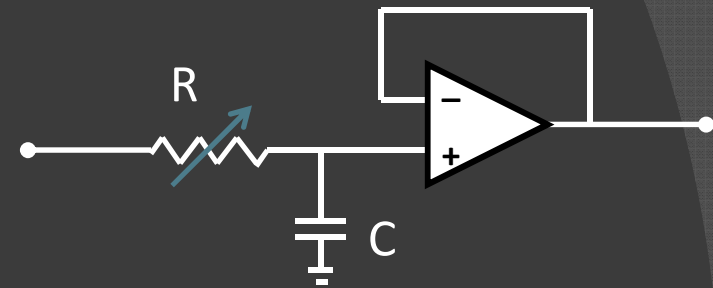
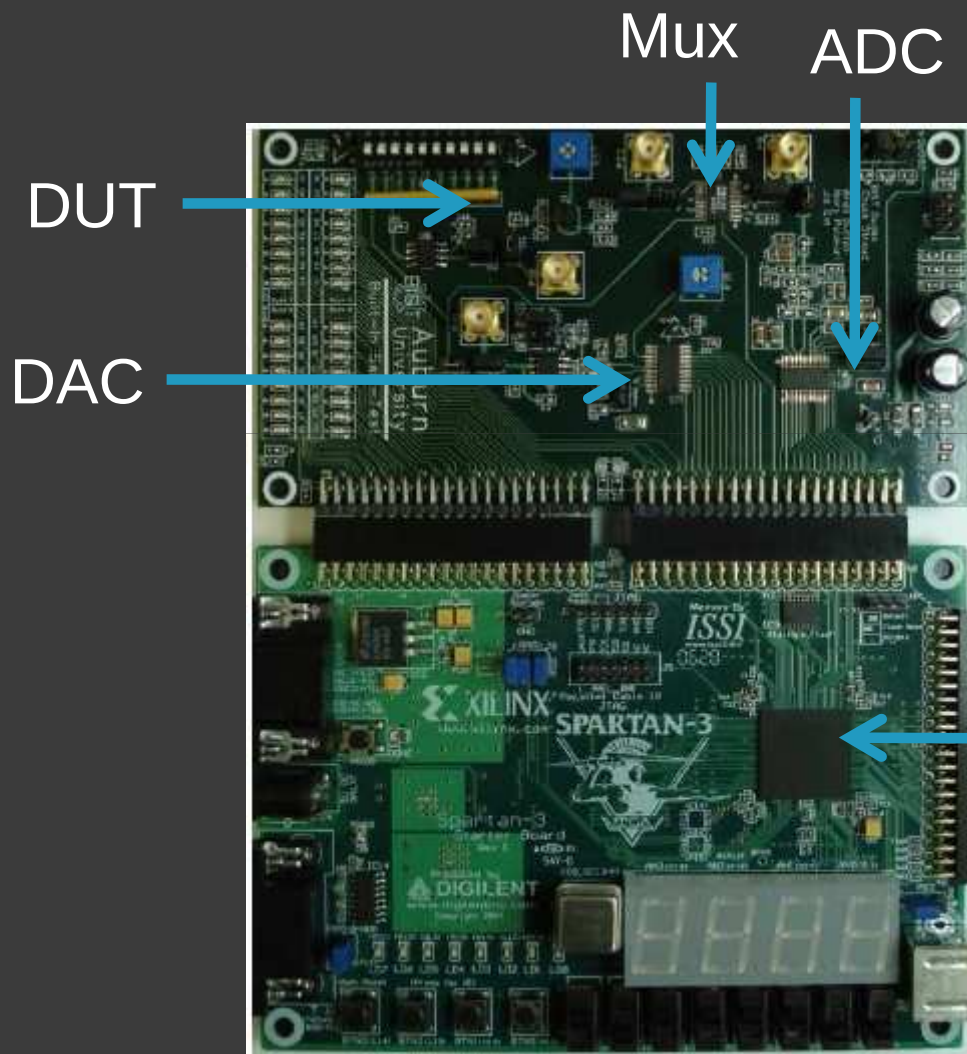
VHDL Generation Options



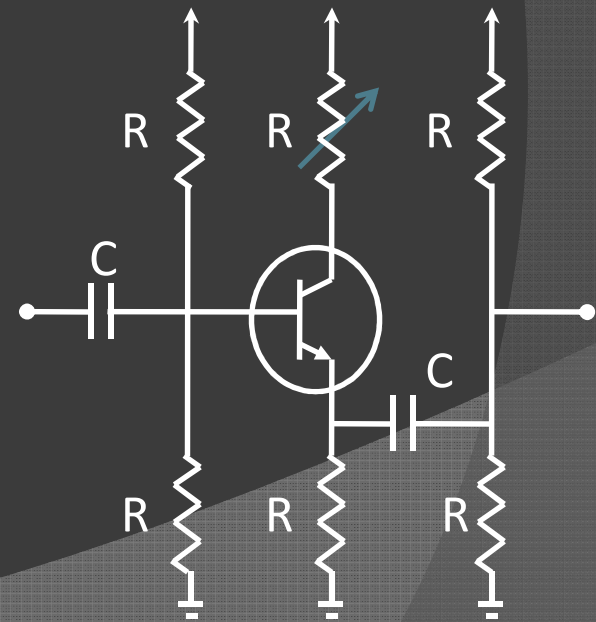
VHDL Generation Options



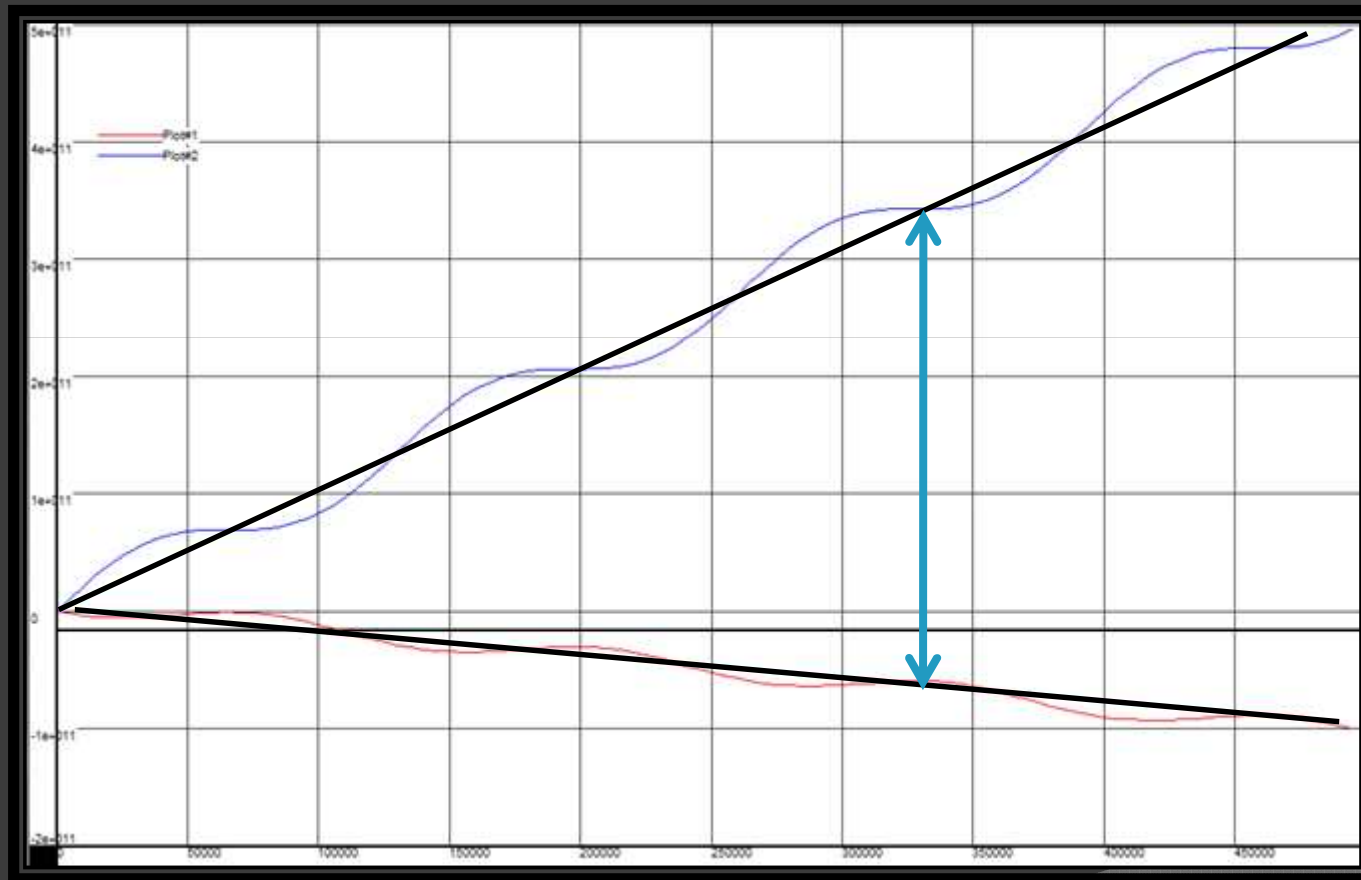
Example Implementations



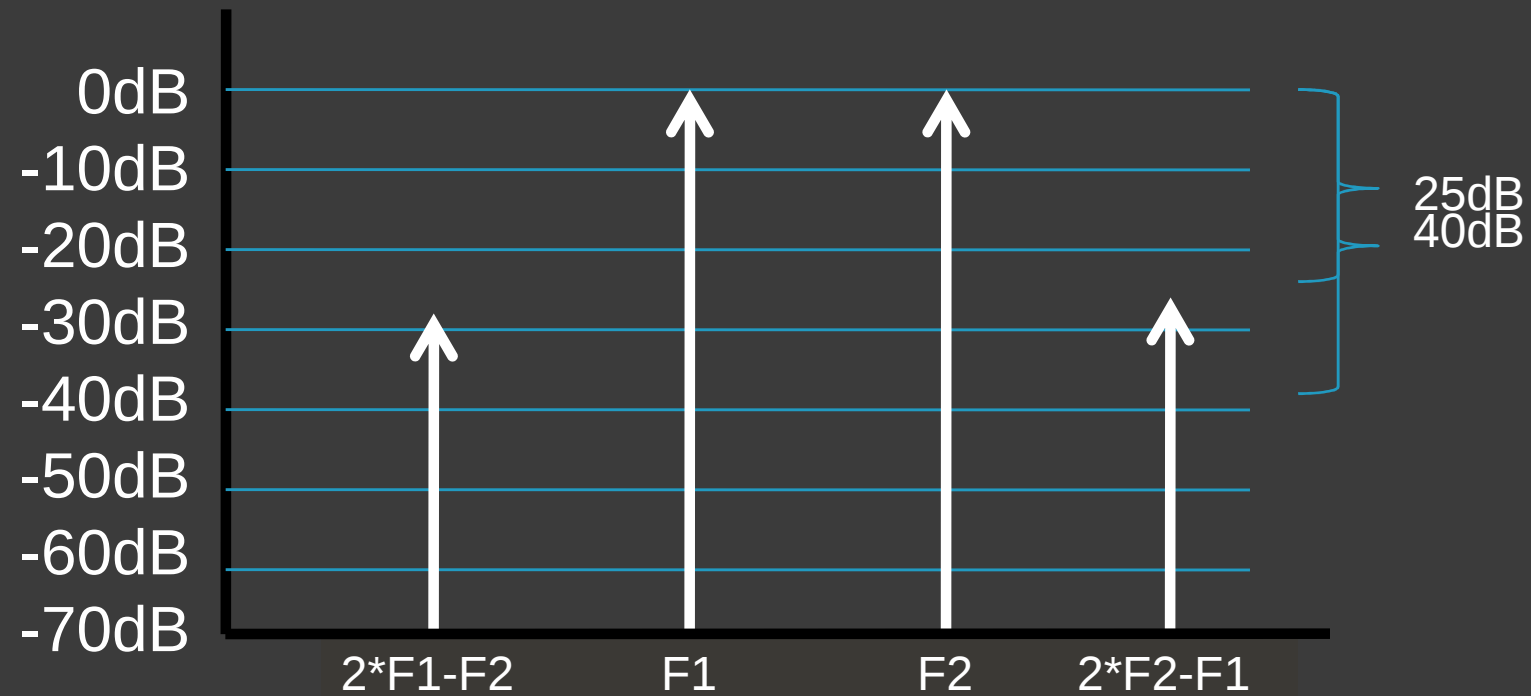
FPGA
TPG
ORA



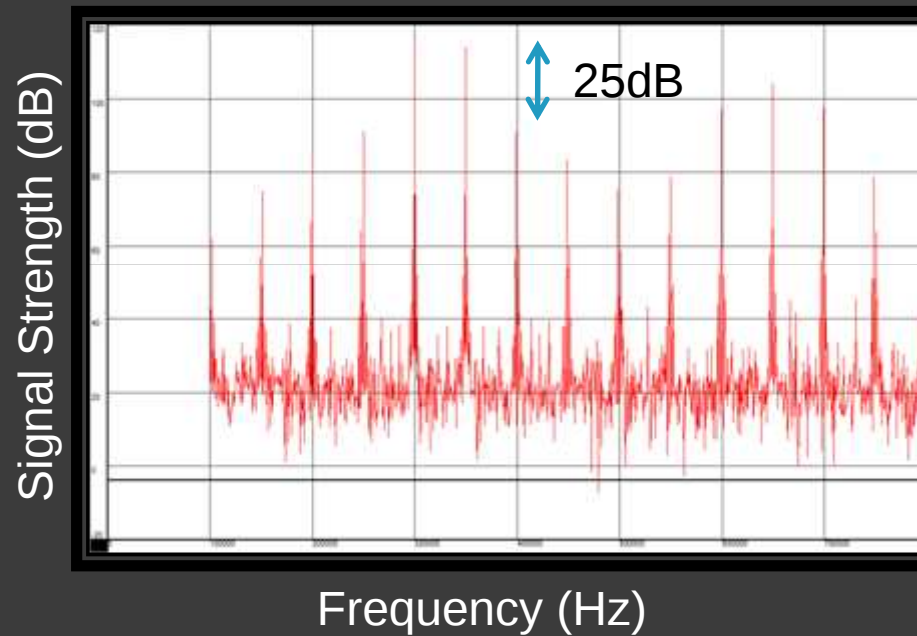
ORA Accumulators



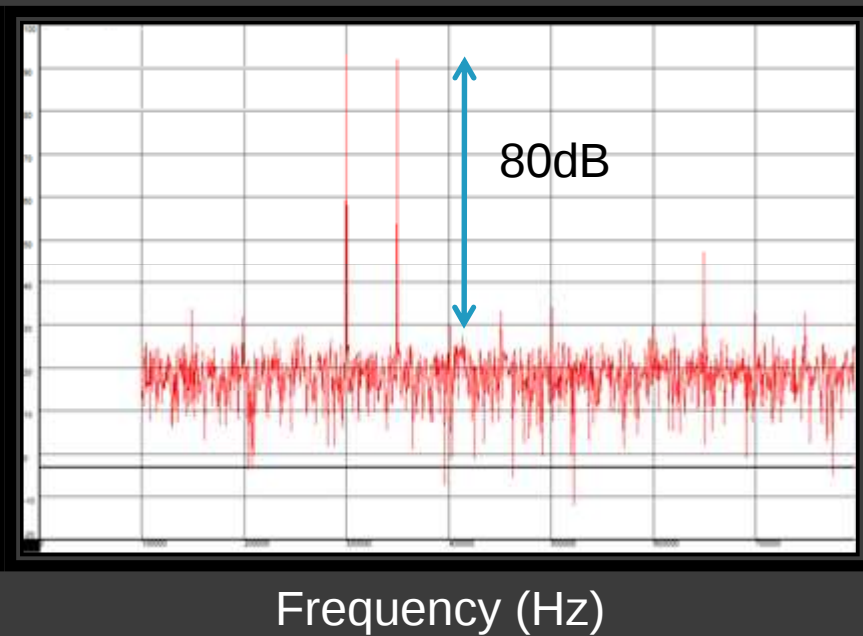
Linearity Measurement



Linearity

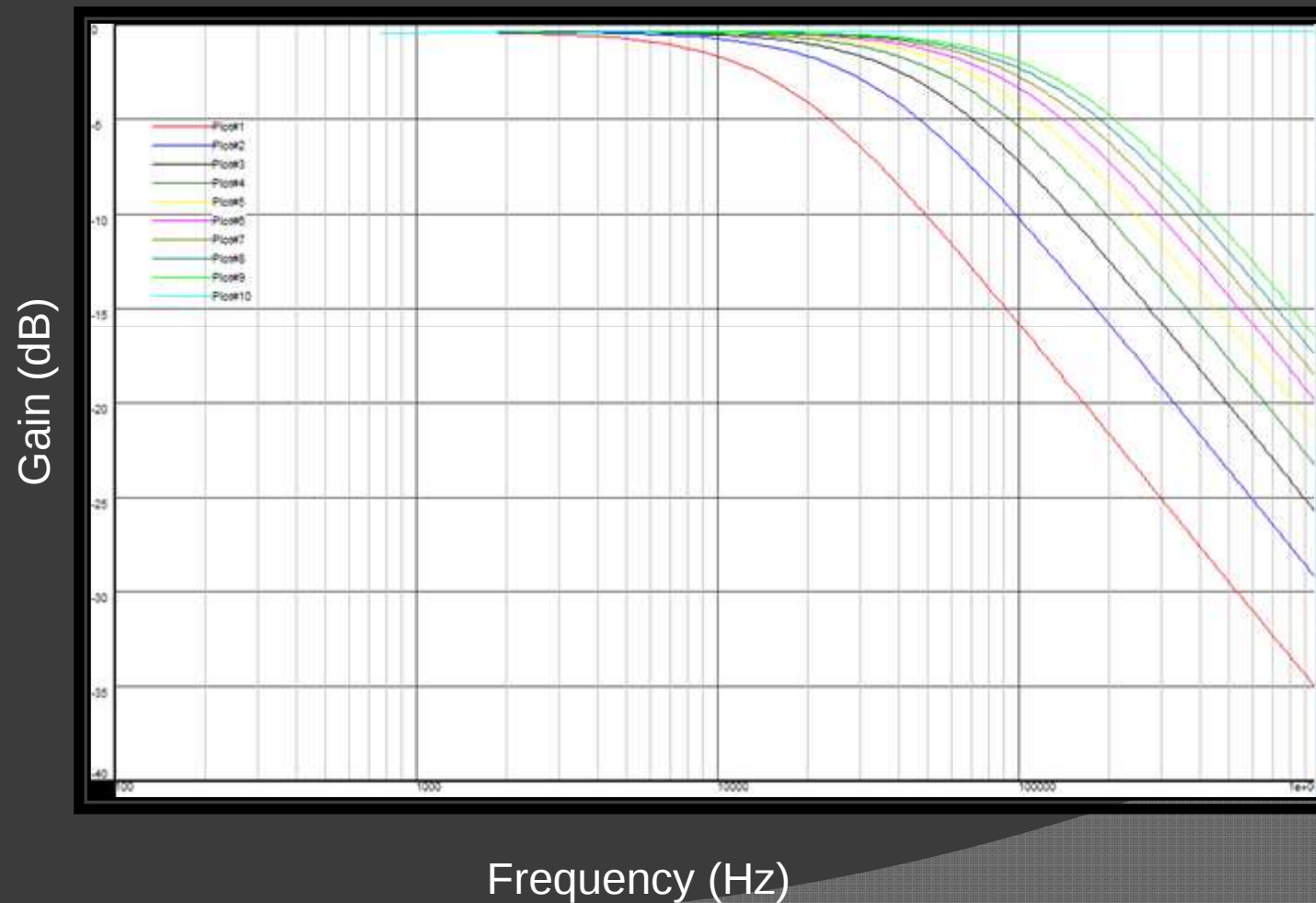


Very Non-Linear System

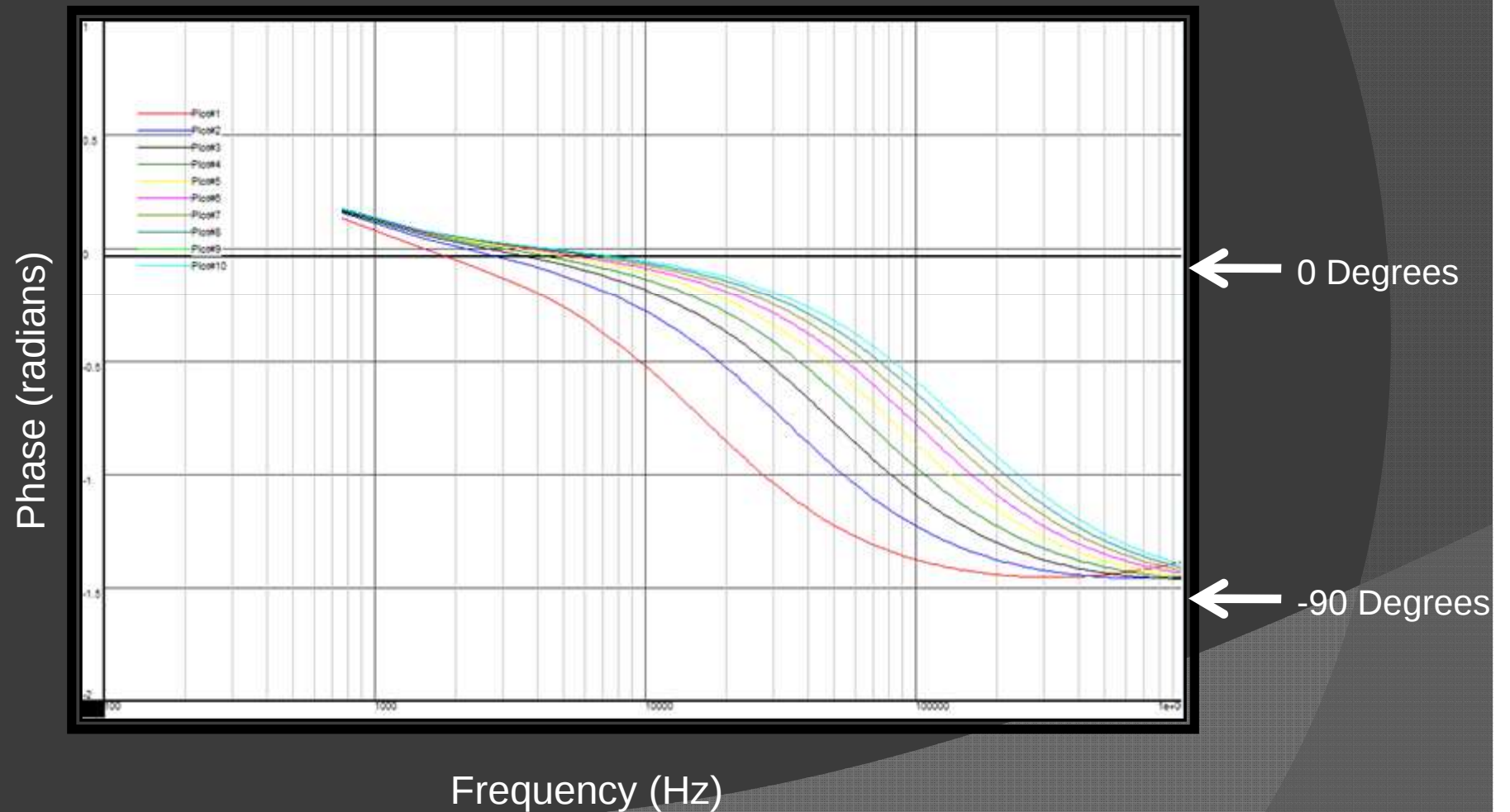


Linear System

Frequency Response - Gain

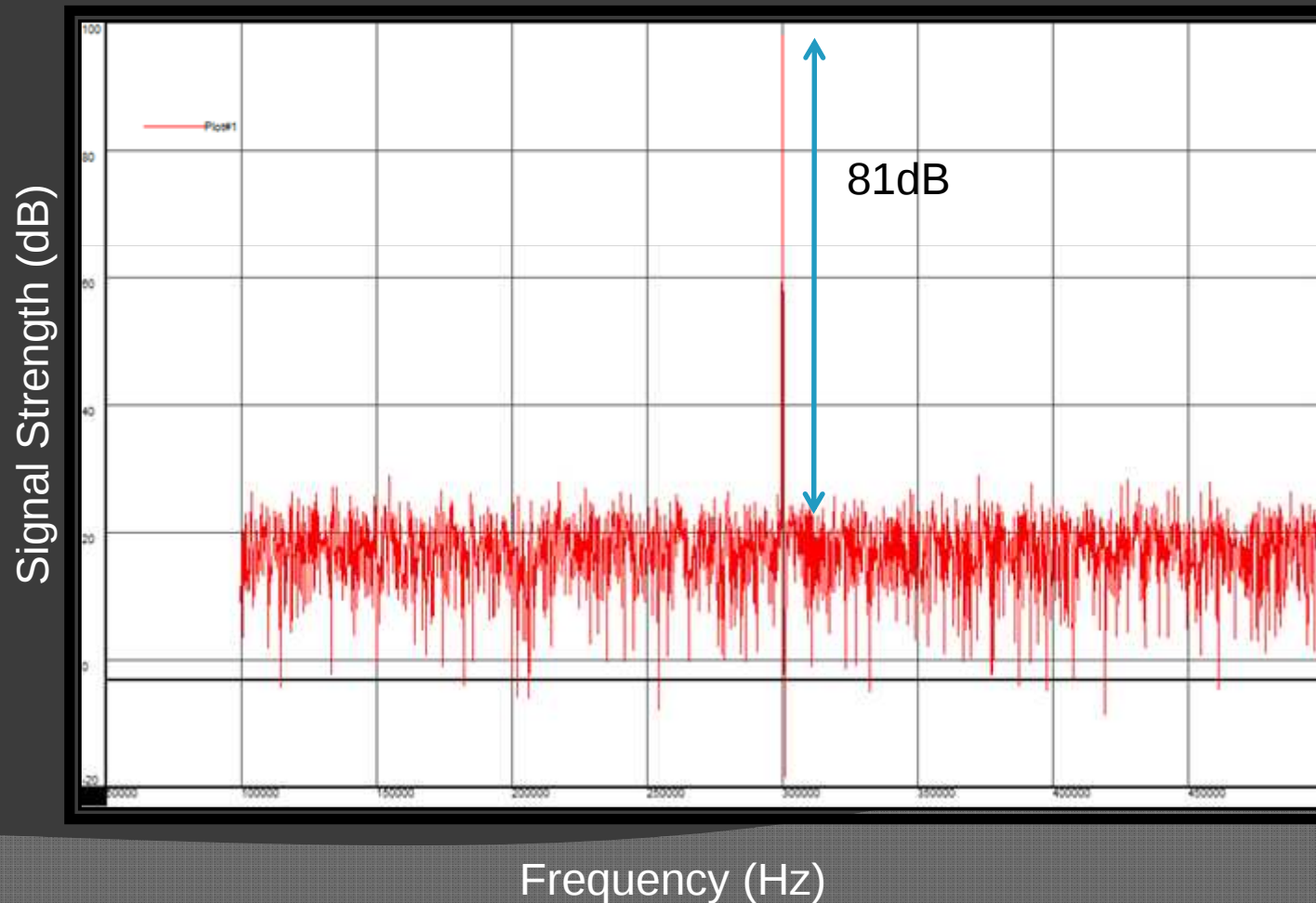


Frequency Response -Phase



Noise Figure

$$\text{NoiseFigure} = 10 * \log\left(\frac{\text{SNR}_{in}}{\text{SNR}_{out}}\right) = \text{SNR}_{in}(\text{db}) - \text{SNR}_{out}(\text{db})$$



$\text{SNR}_{IN} = 109\text{dB}$
 $\text{SNR}_{OUT} = 81\text{dB}$
 $\text{NF} = 28\text{dB}$

RunTime=0.52s

Summary

- ⦿ Capability to measure
 - Linearity
 - Frequency Response
 - Noise Figure
- ⦿ Automatic Generation of VHDL
 - Overcome lack of VHDL trigonometric functions
 - Implementation in any mixed-signal system
 - FPGA and ASIC
- ⦿ Fast & accurate measurements compared to external test equipment

Questions?